VERSION WITH MARKINGS TO SHOW CHANGES MADE

1. (TWICE AMENDED) An apparatus comprising:

an input section configured to generate a first control signal and a second control signal in response to an input signal and a select signal, wherein said input section comprises a first device and a second device each having a source and a drain configured to connect said input signal with said first control signal and said second control signal in response to said select signal; and

an output section configured to generate an output signal in response to said first and said second control signals, wherein said output signal is (i) related to said input signal when in a first mode and (ii) disabled when in a second mode, wherein one or more third devices each have a source and a drain configured to connect said first control signal and said second control signal when in said first mode.

8. (AMENDED) The apparatus according to claim 1, further [A multiplexer or Programmable Interconnect Matrix] comprising two or more of each of said [apparatus of claim 1] input section or said output section, configured as a multiplexer or a programmable interconnect matrix.

10. (AMENDED) The apparatus according to claim 1, wherein said first and said second modes are controlled by said first and said second control signals.

11. (TWICE AMENDED) The apparatus according to claim 1, wherein said input section further comprises:

[one or more second devices; and]

one or more [third] fourth devices coupled to said first and said second devices and configured to generate said first and said second control signals.

12. (TWICE AMENDED) The apparatus according to claim 11, wherein:

[said one or more second devices are coupled to said input signal and configured in response to said select signal; and]

said one or more [third] fourth devices are coupled to (i) said select signal and (ii) a supply voltage or a ground voltage.

13. (TWICE AMENDED) The apparatus according to claim 12, wherein said output section comprises:

one or more [fourth] fifth devices; and

one or more [fifth] sixth devices, wherein said [fourth and] fifth and said sixth devices are configured to present said

output signal in response to said first and said second control signals.

15. (TWICE AMENDED) An apparatus comprising:

means for generating a first control signal and a second control signal in response to an input signal and a select signal, wherein said input signal is connected to said first and said second control signals in response to a first state of said select signal; and

means for generating an output signal in response to said first and said second control signals, wherein said output signal is (i) related to said input signal when in a first mode and (ii) disabled when in a second mode, wherein one or more devices each have a source and a drain configured to connect said first control signal and said second control signal when in said first mode.

16. (TWICE AMENDED) A method for tri-stating an output of a bit, comprising the steps of:

(A) generating [a first state of] said output [by tracking an input when in a first mode] in response to a first control signal and a second control signal;

(B) [generating a second state of said output] connecting an input to said first and second control signals when in a [second] first mode; and

(C) isolating said [output] first and said second control signals from said input when in [said] a second mode, wherein one or more first devices each have a source and a drain configured to connect said first control signal and said second control signal when in said first mode.

17. (TWICE AMENDED) The method according to claim 16, wherein [step (A)] said connecting step further comprises:

turning on one or more second devices; and

turning off one or more third devices.

18. (TWICE AMENDED) The method according to claim 17, wherein [step (B)] said isolating step further comprises:

turning on said one or more [fourth] third devices; and

turning off said one or more [fifth] first and said one or more second devices.

21. (AMENDED) The apparatus according to claim 1, wherein said output signal [follows] tracks said input signal [without a voltage difference due to a threshold of a second one or more devices] and swings from rail to rail.

R E M A R K S

Careful review and examination of the subject application are noted and appreciated.

In one embodiment, the presently claimed invention provides an apparatus comprising an input section and an output section. The input section may be configured to generate a first control signal and a second control signal in response to an input signal and a select signal. The output section may be configured to generate an output signal in response to the first and the second control signals. The input section generally comprises a first device and a second device. The first and the second devices each have a source and a drain configured to connect the input signal with the first control signal and the second control signal in response to the select signal. The output signal is generally (i) related to the input signal when in a first mode and (ii) disabled when in a second mode. One or more third devices each having a source and a drain may be configured to connect the first control signal and the second control signal when in the first mode.

SUPPORT FOR CLAIM AMENDMENTS

Support for the amendments to the claims can be found in the drawings as originally filed, for example, in FIGS. 5 and 6, and in the specification as originally filed, for example, on page

6, lines 12-18, on page 8, lines 1-9, and on page 10, line 11 through page 13, line 15. As such, no new matter has been added.

IN THE DRAWINGS

New drawings for FIGS. 1-3 including the changes approved by the Examiner in the Office Action dated December 4, 2002 are submitted herewith.

CLAIM OBJECTIONS

The objection to claim 8 under 37 CFR 1.75(c) has been obviated by appropriate amendment and should be withdrawn.

CLAIM REJECTIONS UNDER 35 U.S.C. §102

The rejection of claims 1-7 and 9-21 under 35 U.S.C. §102(e) as being anticipated by Hanson et al. '165 (hereinafter Hanson) has been obviated by appropriate amendment and should be withdrawn.

Hanson is directed to reduced voltage input/reduced voltage output tri-state buffers (Title).

In contrast, the present invention (claim 1) provides an input section configured to generate a first control signal and a second control signal in response to an input signal and a select signal. The input section comprises a first and a second device each having a source and a drain configured to connect the input

signal with the first control signal and second control signal, respectively, in response to the select signal. One or more third devices each have a source and a drain configured to connect the first control signal and the second control signals when in a first mode. Claims 15 and 16 include similar recitations. Hanson does not disclose or suggest each and every element of the presently claimed invention, arranged as in the present claims. As such, the presently claimed invention is fully patentable over Hanson and the rejection should be withdrawn.

Specifically, assuming, *arguendo*, the signals 406 and 404 in FIG. 6 of Hanson are similar to the presently claimed first and second control signals (as suggested on page 3, paragraph no. 4, lines 4-5 and for which Applicants' representative does not necessarily agree), Hanson does not disclose or suggest a first device and a second device each having a source and a drain configured to connect the input signal with the first and second control signals, as presently claimed. In particular, the input signal IN of Hanson is connected to a first source/drain of the devices N1 and N2 (see FIG. 6 of Hanson). A second source/drain of the devices N1 and N2 do not connect to the signals 406 and 404 (see FIG. 6 of Hanson). Instead, Hanson discloses the second source/drains of the devices N1 and N2 drive gates of the transistors P2 and N3 (see FIG. 6 of Hanson). Further evidence that Hanson does not disclose or suggest a first device and a

second device each having a source and a drain configured to connect the input signal with the first and second control signals, as presently claimed, is provided by transistors N1, N2, N3 and P3 in FIGS. 4, 7, 10, 11, 12; transistors X1, N2, N3 and P3 in FIG. 5; transistors N2, N3(sic, N1), N3 and P3 in FIG. 8; transistors N3(sic, N1), N7(sic, N2), N3 and P3 in FIG. 9. Thus, Hanson does not disclose a first device and a second device configured to connect the input signal to the first and second control signals, as presently claimed. Therefore, Hanson does not disclose each and every element of the presently claimed invention, arranged as in the present claims. As such, the presently claimed invention is fully patentable over the cited reference and the rejection should be withdrawn.

Claims 2-14 and 17-21 depend, either directly or indirectly, from claims 1 or 16 which are believed to be allowable. As such, the presently claimed invention is fully patentable over the cited reference and the rejection should be withdrawn.

Accordingly, the present application is in condition for allowance. Early and favorable action by the Examiner is respectfully solicited.

The Examiner is respectfully invited to call the Applicants' representative should it be deemed beneficial to further advance prosecution of the application.

If any additional fees are due, please charge our office Account No. 50-0541.

Respectfully submitted,

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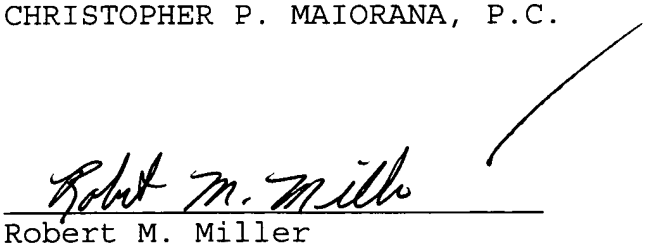

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